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PATENT ABSTRACTS OF JAPAN

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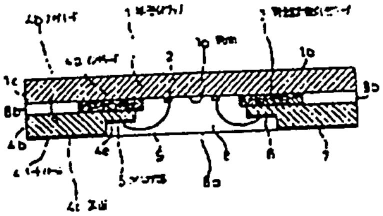
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To make a package small in thickness in a CSP (Chip Scale Package) structure by which a lead frame of the same size is mounted on a semiconductor chip.
SOLUTION: A lead frame 4 to be adhered to a semiconductor chip 1 is almost the same in size as the chip 1. The surface 4e of an inner lead 4a of the lead frame 4 is coined to form a coined part 5 with reduced thickness. The lead frame 4 and the end surface 1c of the chip 1 are adhered to each other with a double-faced adhesive tape 3 interposed. The coined part 5 of the inner lead 4a is connected with a bonding pad 2 of the chip 1 through a bonding wire 9. The surface 1a of the chip 1 is packaged with a mold resin 8, thereby exposing only the surface 4c of an outer lead 4b on the packaged resin surface 8a.



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CLAIMS

[Claim(s)]

[Claim 1] Pile up the leadframe of a semiconductor chip and abbreviation same size on the surface of a semiconductor chip, and it sticks through adhesives. Connect the inner lead and semiconductor chip of a leadframe by the bonding wire, and the front-face side of a semiconductor chip is closed by the mould resin so that it may become flat-tapped with the front face of an outer lead. In the semiconductor device which exposed the front face of an outer lead on the closure resin front face The semiconductor device characterized by having reduced the thickness by the side of the front face of an inner lead, and making an inner lead front face lower one step than an outer lead front face so that the bonding wire connected to an inner lead may not cross the front face of an outer lead.

[Claim 2] The semiconductor device according to claim 1 which also closed the gap between the end faces which form the size of the above-mentioned leadframe a little more greatly than a semiconductor chip, and are formed when this leadframe is piled up on the surface of a semiconductor chip by the mould resin.

[Claim 3] The semiconductor device according to claim 1 or 2 which made the adhesives which stick a leadframe on the front face of the above-mentioned semiconductor chip placed not only between an inner lead side but between outer lead sides.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]
[The technical field to which invention belongs] the semiconductor device with which this invention used the leadframe -- starting -- especially, a chip size and abbreviation -- it is related with a thin shape and small semiconductor package structure with the same size

[0002]
[Description of the Prior Art] Although the LOC (Lead On Chip) structure which can contain the semiconductor chip which turned into the comparatively small package on a large scale is adopted in mass DRAM (Dynamic Random Access Memory) corresponding to the demand of high density assembly, the package further miniaturized by even chip size level by the increase in capacity has come to be required. Moreover, it is required that the semiconductor package for electronic equipment should also be miniaturized more with reduction of sizes, such as a personal computer, facsimile, personal telephone, and an IC card. And only the area which a package only has chiefly is called for also in the thickness direction of a package rather than it is asked for this miniaturization.

[0003] Conventionally, the semiconductor device called CSP (Chip Scale Package) which exposed a part of lead on the base of a package as what responds to these requests is proposed (JP,6-132453,A). Specifically, as shown in drawing 7 , an end face is doubled and the leadframe 22 of the same size as a semiconductor chip 21 is stuck on wiring side (front face) 21a of a semiconductor chip 21 with adhesives 23. In case it closes by the mould resin 25 after connecting inner lead 22a of a leadframe 22, and a semiconductor chip 21 by the bonding wire 24, the front-face side of a semiconductor chip 21 is closed by the mould resin 25, and surface 22c of outer lead 22b is exposed to surface 25a of the mould resin 25.

[0004] Although the bonding wire 24 which connects inner lead 22a and a semiconductor chip 21 needs to prepare a level difference here at a lead from surface 25a of the mould resin 25 made flat-tapped with surface 22c of outer lead 22b so that it may not disturb, in this conventional example, inner lead 22a is made lower one step than outer lead 22b by carrying out down set processing of the leadframe 22.

[0005]
[Problem(s) to be Solved by the Invention] By it, the miniaturization of a package is not only reflected in the area which a package has chiefly by the conventional technology mentioned above, but has come to be reflected also in the thickness direction of a package. However, since it is made to prepare a level difference in a lead by carrying out down set processing of the leadframe, the processing depth beyond lead ** is needed, and the part and package thickness cannot be made thin.

[0006] moreover -- although the minimum package can be obtained as the size of a package is the same as that of a semiconductor chip 1 -- dispersion in the size of a semiconductor chip 1 -- the time of a mould resin seal -- a mould -- there is a possibility that metal mold may damage a part of semiconductor chip 1

[0007] Furthermore, since adhesion fixation of the leadframe to a semiconductor chip was performed only by the inner lead side, although the case where fixation in the thickness direction by the side of an outer lead was not enough arose on the occasion of a mould resin seal, when

fixation was not enough, a mould resin needed to begin to delete a wraparound and a front face thinly on the surface of the outer lead.
[0008] The purpose of this invention is to cancel the trouble of the conventional technology mentioned above and offer the semiconductor device which can make package thickness thinner. Moreover, the purpose of this invention is at the time of a mould resin seal to offer the semiconductor device which a semiconductor chip does not damage. Furthermore, the purpose of this invention is after a mould resin seal to offer the semiconductor device which does not need shaving **** on the front face of an outer lead.

[0009]
[Means for Solving the Problem] The semiconductor device of this invention piles up the leadframe of a semiconductor chip and abbreviation same size on the surface of a semiconductor chip, and sticks it through adhesives. Connect the inner lead and semiconductor chip of a leadframe by the bonding wire, and the front-face side of a semiconductor chip is closed by the mould resin so that it may become flat-tapped with the front face of an outer lead. In the semiconductor device which exposed the front face of an outer lead on the closure resin front face The thickness by the side of the front face of an inner lead is reduced, and one step of inner lead front face is made lower than an outer lead front face so that the bonding wire connected to an inner lead may not cross the front face of an outer lead. Thus, if the thickness of an inner lead is reduced rather than an outer lead and it can be made to make an inner lead lower one step than an outer lead, as compared with the case where the down set of the lead is carried out, package thickness can be made thinner.

[0010] Moreover, in the semiconductor device of such this invention, also closing the gap between the end faces which form the size of a leadframe a little more greatly than a semiconductor chip, and are formed when a leadframe is piled up on the surface of a semiconductor chip by the mould resin can prevent breakage of a semiconductor chip effectively. Moreover, making the adhesives which stick a leadframe on the surface of a semiconductor chip placed not only between an inner lead side but between outer lead sides can prevent the wraparound of the mould resin to the front face of an outer lead.

[0011]
[Embodiments of the Invention] The gestalt of operation of the semiconductor device of this invention is explained in detail using a drawing below. Drawing 1 is the cross section of CSP structure which carried the leadframe 4 of the same size on the semiconductor chip 1.

[0012] Near the center of surface 1a which is the wiring side, a bonding pad 2 is arranged and a semiconductor chip 1 is constituted. The leadframe 4 stuck on surface 1a of this semiconductor chip 1 consists of same sizes as a semiconductor chip 1, and has inner lead 4a for connecting with a semiconductor chip 1, and outer lead 4b used as an external terminal. The attachment by the semiconductor chip 1 and the leadframe 4 piles up a semiconductor chip 1 and a leadframe 4, and is performed through the tape 3 with double-sided adhesives so that end-face 1c of a semiconductor chip 1 and 4d of end faces of a leadframe 4 may be in agreement.

[0013] Instead of having not bent, a leadframe 4 reduces a part of thickness, and has made it thin. That is, inner lead 4a of a leadframe 4 forms the coining section 5 which carried out coining of the attachment side and opposite side (surface 4e) side, and made it thinner than outer lead 4b, and the height of the bonding wire 9 which connects inner lead 4a and the bonding pad 2 of a semiconductor chip 1 is made to become lower than the attachment side and opposite side (surface 4c) of outer lead 4b.

[0014] Thus, the bonding pad 2 allotted near [where silver plating 6 was performed to the coining section 5 of inner lead 4a which reduced thickness and was made lower one step than surface 4c of outer lead 4b, and silver plating 6 was performed] the center of the coining section 5 and a semiconductor chip 1 is connected by the bonding wire 9. Since one step of coining section 5 is low, the height of a bonding wire 9 can be stopped lower than surface 4c of outer lead 4b.

[0015] Closure by the mould resin 8 is performed by the surface 1a side of a semiconductor chip 1. Thickness of the mould resin 8 is made into the same height as surface 4c of outer lead 4b, and although inner lead 4a, a bonding wire 9, etc. are buried and protected in the mould resin 8, surface

4c of outer lead 4b is exposed to closure resin surface 8a. At this time, it is small in the area of a package, and in order to make thickness of a package thin, it is made for the mould resin 8 not to have the surroundings top in rear-face 1b of the end-face 1c and the semiconductor chip 1 of 4d of end faces of a leadframe 4, and a semiconductor chip 1.

[0016] Thus, since the constituted semiconductor package has prepared the level difference in the lead with coining, it does not need to carry out the down set of the leadframe like before. Moreover, package thickness turns into thickness which totaled the semiconductor thickness of tip, tape ** with double-sided adhesives, and lead ** of one sheet, and since the processing depth more than the double precision of lead ** which a down set requires is not required of a lead portion, it can make thickness of a package thinner.

[0017] In order to manufacture the semiconductor package mentioned above, in order to make end-face 8b of the mould resin 8 in agreement with end-face 1c of a semiconductor chip 1, the leadframe 4 used for a package is first constituted so that the position of the resin dambar 17 may be arranged along with the periphery of the semiconductor chip 1 shown with the alternate long and short dash line, as shown in drawing 2 . moreover, the mould used at the time of package manufacture -- metal mold is made into the almost same size as the appearance of a semiconductor chip 1, and as the mould resin 8 does not turn around it to the rear-face 1b side of a semiconductor chip 1, it carries out the mould only of the front-face side of a semiconductor chip In addition, 4d of end faces of a leadframe 4 turns into a cutting plane of the resin dambar 17.

[0018] Metal mold cuts the resin dambar 17 after a mould, and Leads 4a and 4b are separated separately. Here, before cutting the resin dambar 17, it is good that wetting with solder performs good silver plating 7 to surface 4c of outer lead 4b exposed to surface 8a of the mould resin 8 simultaneously with the silver plating 6 of the coining section 5 of inner lead 4a. If it carries out like this, it becomes unnecessary, and the sheathing solder plating of the front face of outer lead 4b is advantageous after a mould also at the point that the process which gives a damage to a package can be reduced while it can carry out cost reduction.

[0019] According to this manufacture method, remaining as it is or since it can omit a part and can use, though it is equivalent in price as compared with the conventional mould package in the manufacturing process and resin mould process of the LOC leadframe currently performed conventionally, the package of small and a thin shape can be obtained more.

[0020] since [by the way,] the size of a package is the same as that of a semiconductor chip 1 in the mould field of the package structure shown in drawing 1 -- dispersion in the size of a semiconductor chip 1 -- a mould -- we are anxious about metal mold damaging a part of semiconductor chip 1 such concern performs a setup to which a mould field is expanded a little to a semiconductor chip 1, as shown in drawing 3 -- it is cancelable namely, the size of a leadframe 4 -- a semiconductor chip 1 -- a little -- large -- forming -- the resin dambar 17 of this leadframe 4 formed a little more greatly -- a mould -- when the size of metal mold is doubled and formed, even if dispersion suits the size of a semiconductor chip 1 -- a mould -- since metal mold stops touching end-face 1c of a semiconductor chip 1, it can prevent breakage of a semiconductor chip 1 In addition, the gap G formed between 4d of end faces of a leadframe 4 and end-face 1c of a semiconductor chip 1 is buried by the mould resin 11 by closure by the mould resin 8. Therefore, end-face 1c of a semiconductor chip 1 is protected by the mould resin 11 after a resin seal.

[0021] Moreover, if the package structure shown in drawing 1 and drawing 3 is not enough as fixation in the thickness direction by the side of outer lead 4b on the tape 3 with double-sided adhesives in case the mould of the package is carried out, a mould resin will need to begin to delete a wraparound and a front face thinly to surface 4c of outer lead 4b. This can prevent effectively surroundings **** to outer lead surface 4c of the mould resin 8 by making the tape 13 with double-sided adhesives with thickness equivalent to the tape 3 with double-sided adhesives by the side of an inner lead intervene between the semiconductor chip 1 near the package periphery, and outer lead 4b, as shown in drawing 4 . In addition, of course, it is good also as structure which combined drawing 3 and drawing 4 .

[0022] Moreover, with the structure of drawing 1 , drawing 3 , and drawing 4 , although silver plating 7 was performed all over surface 4c of outer lead 4b, if it does so, it will be expected that the silver amount of eyes increases and cost goes up. However, as shown in drawing 5 , by making small the field of the silver plating 14 of outer lead 4b, it can decrease and the silver amount of eyes can be made advantageous in cost. In addition, a sign 15 shows the portion which has not performed silver plating.

[0023] Drawing 6 shows the example which carried out sheathing of the solder plating 16 to surface 4c of outer lead 4b. Although it means that the process of carry out [to the front face of outer lead 4b / sheathing of the solder plating] which gives a damage after a mould to a package increases as mentioned already, this invention does not eliminate this.

[0024] In the gestalt of this operation described above, the thickness of 0.3mm and a leadframe of the thickness of the used semiconductor chip is 0.05mm of ****** of 0.15mm and a tape with double-sided adhesives. Moreover, 0.075mm coining was performed to the inner lead. Moreover, although the coining method was used as the technique of reducing the thickness of an inner lead with the gestalt of this operation, you may use the half dirty method. Moreover, although the tape with double-sided adhesives was used as a means to stick a leadframe on a semiconductor chip, it is only good also as adhesives.

[0025]

[Effect of the Invention] Since the level difference was prepared in the lead by reducing the thickness of an inner lead according to this invention and the processing depth beyond lead ** is not needed like the conventional example which prepared the level difference by carrying out down set processing, package thickness can be made thinner. moreover -- since the size of a leadframe was formed a little more greatly than a semiconductor chip -- a mould -- the injury on the semiconductor chip by metal mold can be prevented effectively Furthermore, since it was made to make the adhesives which stick a leadframe on the surface of a semiconductor chip placed also between outer lead sides, the wraparound of the mould resin on the front face of an outer lead can be prevented, and surface shaving **** is not required.

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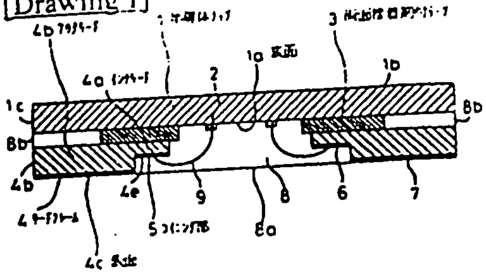
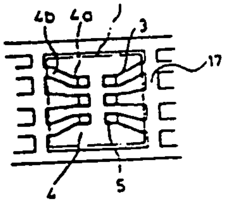
DRAWINGS

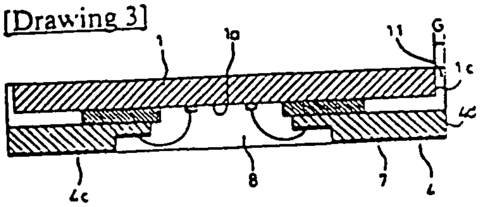
[Drawing 1]



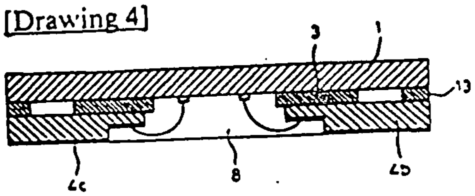
[Drawing 2]



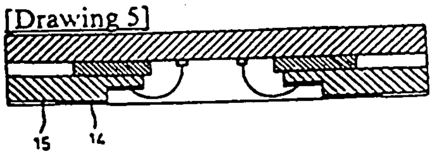
[Drawing 3]



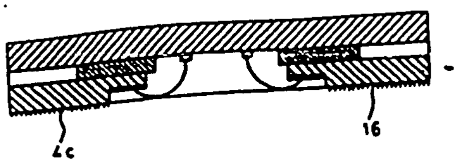
[Drawing 4]



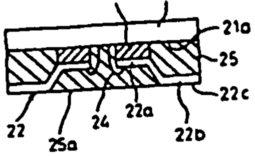
[Drawing 5]



[Drawing 6]



[Drawing 7]



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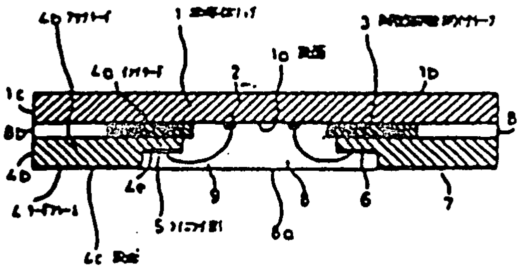
最終頁に続く

(54)【発明の名称】半導体装置

(57)【要約】
【課題】半導体チップの上に同一サイズのリードフレームを載せるCSP（ChipScale Package）構造において、パッケージ厚さをより薄くする。

【解決手段】半導体チップ1に貼り付けるリードフレーム4は、半導体チップ1と略同一サイズとする。リードフレーム4のインナリード4aの表面4eにコイニングを施して厚みを減らしたコイニング部5を形成する。両面接着用絶縁テープ3を介してリードフレーム4と半導体チップ1とを端面4d、1cを合わせて貼り付ける。インナリード4aのコイニング部5と半導体チップ1のボンディングパッド2とをボンディングワイヤ9で接続する。半導体チップ1の表面1aにモールド樹脂8を封止し、封止樹脂表面8aにアウタリード4bの表面4cのみを露出させる。



【特許請求の範囲】

【請求項1】半導体チップの表面に半導体チップと略同一サイズのリードフレームを重ね合わせて接着剤を介して貼り付け、リードフレームのインナリードと半導体チップとをボンディングワイヤで接続し、アウタリードの表面と面一となるように半導体チップの表面側をモールド樹脂で封止して、封止樹脂表面にアウタリードの表面を露出させた半導体装置において、インナリードに接続されるボンディングワイヤがアウタリードの表面を越えないように、インナリードの表面側の厚みを減らしてインナリード表面をアウタリード表面より一段低くしたことを特徴とする半導体装置。

【請求項2】上記リードフレームのサイズを半導体チップよりやや大きめに形成し、該リードフレームを半導体チップの表面に重ね合わせたとき形成される端面間のギャップもモールド樹脂で封止するようにした請求項1に記載の半導体装置。

【請求項3】上記半導体チップの表面にリードフレームを貼り付ける接着剤を、インナリード側のみならずアウタリード側にも介在させた請求項1または2に記載の半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明はリードフレームを使用した半導体装置に係り、特にチップサイズと略同一のサイズをもつ薄型かつ小型の半導体パッケージ構造に関するものである。

【0002】

【従来の技術】大容量のＤＲＡＭ（Dynamic Random Access Memory）では、高密度実装の要求に対応して、比較的小さなパッケージに大形化した半導体チップを収納できるＬＯＣ（Lead On Chip）構造が採用されているが、容量の増加により更にチップサイズレベルにまで小形化されたパッケージが要求されるようになってきた。また、電子機器用の半導体パッケージも、パソコン、ファックス、パーソナル電話機、ＩＣカード等のサイズの縮小に伴って、より小形化することが要求されている。しかも、この小形化は、単にパッケージの専有する面積にのみ求められるのではなく、パッケージの厚さ方向にも求められている。

【0003】従来、これらの要請に応えるものとして、リードの一部のみをパッケージの底面に露出させたＣＳＰ（Chip Scale Package）と呼ばれる半導体装置が提案されている（特開平6－132453号公報）。具体的には、図7に示すように、半導体チップ21の回路面（表面）21ａに半導体チップ21と同一サイズのリードフレーム22を両面を合わせて接着剤23で貼り付ける。リードフレーム22のインナリード22ａと半導体チップ21とをボンディングワイヤ24で接続した後、モールド樹脂25で封止する際、半導体チップ21の表面側をモールド樹脂25で封止して、モールド樹脂25の表面25ａにアウタリード22ｂの表面22ｃを露出させたものである。

【0004】ここに、インナリード22ａと半導体チップ21とを接続するボンディングワイヤ24が、アウタリード22ｂの表面22ｃと面一にしたモールド樹脂25の表面25ａからはみださないように、リードに段差を設ける必要があるが、この従来例では、リードフレーム22をダウンセット加工することによって、インナリード22ａをアウタリード22ｂよりも一段低くしている。

【0005】

【発明が解決しようとする課題】上述した従来技術によって、パッケージの小形化は、パッケージの専有する面積に反映されるばかりでなく、パッケージの厚さ方向にも反映されるようになってきた。しかし、リードフレームをダウンセット加工することによってリードに段差を設けるようにしているので、リード厚を超えた加工深さが必要となり、その分、パッケージ厚さを薄くできない。

【0006】また、パッケージのサイズが半導体チップ1と同一であると、最小のパッケージを得ることができるが、半導体チップ1の大きさのばらつきによっては、モールド樹脂封止時にモールド金型が半導体チップ1の一部を破損してしまうおそれがある。

【0007】さらに、半導体チップへのリードフレームの接着固定は、インナリード側のみで行なっているため、モールド樹脂封止の際に、アウタリード側の厚み方向での固定が十分でない場合が生じるが、固定が十分でないと、アウタリードの表面にモールド樹脂が薄く回り込み、表面を削り出す必要があった。

【0008】本発明の目的は、上述した従来技術の問題点を解消して、パッケージ厚さをより薄くできる半導体装置を提供することにある。また、本発明の目的は、モールド樹脂封止時、半導体チップが破損しない半導体装置を提供することにある。さらに、本発明の目的は、モールド樹脂封止後、アウタリード表面の削り出しを必要としない半導体装置を提供することにある。

【0009】

【課題を解決するための手段】本発明の半導体装置は、半導体チップの表面に半導体チップと略同一サイズのリードフレームを重ね合わせて接着剤を介して貼り付け、リードフレームのインナリードと半導体チップとをボンディングワイヤで接続し、アウタリードの表面と面一となるように半導体チップの表面側をモールド樹脂で封止して、封止樹脂表面にアウタリードの表面を露出させた半導体装置において、インナリードに接続されるボンディングワイヤがアウタリードの表面を越えないように、インナリードの表面側の厚みを減らしてインナリード表面をアウタリード表面より一段低くしたものである。こ

のようにインナリードの厚みをアウタリードよりも減らしてインナリードをアウタリードより一段低くできるようにすると、リードをダウンセットする場合に比して、パッケージ厚さをより薄くすることができる。

【0010】また、このような本発明の半導体装置において、リードフレームのサイズを半導体チップよりやや大きめに形成し、リードフレームを半導体チップの表面に重ね合わせたときに形成される端部間のギャップもモールド樹脂で封止することが、半導体チップの損傷を有効に防止できる。また、半導体チップの表面にリードフレームを貼り付ける接着剤を、インナリード側のみならずアウタリード側にも介在させることが、アウタリードの裏面へのモールド樹脂の回り込みを防止できる。

【0011】

【発明の実施の形態】以下に本発明の半導体装置の実施の形態を図面を用いて詳細に説明する。図1は、半導体チップ1上に同一サイズのリードフレーム4を載せたCSP構造の断面図である。

【0012】半導体チップ1は、その配線面である表面1aの中央近傍にボンディングパッド2が配置されて構成される。この半導体チップ1の表面1aに貼り付けられるリードフレーム4は、半導体チップ1と同一サイズで構成され、半導体チップ1と接続するためのインナリード4aと、外部端子となるアウタリード4bとを有する。半導体チップ1とリードフレーム4との貼付けは、半導体チップ1の端面1cとリードフレーム4の端面4dとが一致するように、半導体チップ1とリードフレーム4とを重ね合わせて、両面接着剤付テープ3を介して行う。

【0013】リードフレーム4は折曲していない代りに、一部の厚さを減らして薄くしてある。すなわち、リードフレーム4のインナリード4aは、その貼付け面と反対面（表面4c）側をコイニングしてアウタリード4bよりも薄くしたコイニング部5を形成し、インナリード4aと半導体チップ1のボンディングパッド2とを接続するボンディングワイヤ9の高さをアウタリード4bの貼付け面と反対面（表面4c）よりも低くなるようにしてある。

【0014】このようにして厚さを減らしてアウタリード4bの表面4cよりも一段低くしたインナリード4aのコイニング部5には銀めっき6が施され、銀めっき6が施されたコイニング部5と半導体チップ1の中央近傍に配されたボンディングパッド2とがボンディングワイヤ9によって接続される。コイニング部5が一段低くなっているため、ボンディングワイヤ9の高さは、アウタリード4bの表面4cより低く抑えることができる。

【0015】モールド樹脂8による封止は、半導体チップ1の表面1a側で行なわれる。モールド樹脂8の厚さを、アウタリード4bの表面4cと同一高さにして、インナリード4aおよびボンディングワイヤ9などをモールド樹脂8中に埋めて保護するが、アウタリード4bの表面4cは封止樹脂表面8aに露出させる。このときパッケージの面積を小さく、かつパッケージの厚さを薄くするために、モールド樹脂8は、リードフレーム4の端面4d及び半導体チップ1の端面1c及び半導体チップ1の裏面1bに回りこまないようにする。

【0016】このように構成された半導体パッケージは、コイニングによってリードに段差を設けているため、従来のようにリードフレームをダウンセットする必要はない。また、パッケージ厚さは半導体チップ厚、両面接着剤付テープ厚、及び1枚のリード厚を合計した厚さとなり、ダウンセットが要求するリード厚の2倍以上の加工代がリード部分に要求されないため、パッケージの厚さをより薄くすることができる。

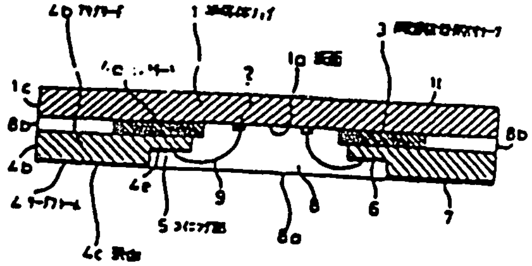
【0017】上記した半導体パッケージを製造するには、まず、モールド樹脂8の端面8bを半導体チップ1の端面1cに一致させるために、パッケージに使用されるリードフレーム4に、その樹脂ダムバー17の位置を、図2に示すように、一点鎖線で示した半導体チップ1の外周に沿って配置するように形成する。また、パッケージ製造時に使用するモールド金型は、半導体チップ1の外形とほぼ同じ大きさとし、半導体チップ1の裏面1b側にモールド樹脂8が回らないようにして、半導体チップの表面側のみをモールドする。なお、リードフレーム4の端面4dは樹脂ダムバー17の切断面となる。

【0018】モールド後、樹脂ダムバー17を金型で切断し、リード4a、4bを個々に切り離す。ここで、樹脂ダムバー17を切断する前に、モールド樹脂8の表面8aに露出するアウタリード4bの表面4cに、半田との濡れが良好なめっき7をインナリード4aのコイニング部5の銀めっき6と同時に行っておくのがよい。こうするとアウタリード4bの表面の外装半田めっきは不要となり、コスト低減できるとともに、モールド後、パッケージにダメージを与える工程を減らすことができる点でも有利である。

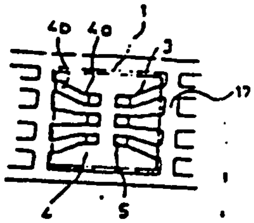
【0019】本製造方法によれば、従来より行われているLOCリードフレームの製造工程、および樹脂モールド工程をそのまま、または、一部変更して利用することができるため、従来のモールドパッケージと比較して低価格に実現でありながら、より小型かつ薄型のパッケージを作ることができる。

【0020】ところで、図1に示すパッケージ構造のモールド構成では、パッケージのサイズが半導体チップ1と同一であるため、半導体チップ1の大きさのばらつきによっては、モールド金型が半導体チップ1の一部を破損してしまうことが懸念される。このような場合には、図3に示すように、半導体チップ1に対してモールド樹脂を若干拡大する設定を行うことによって解消できる。すなわち、リードフレーム4のサイズを半導体チップ1よりやや大きめに形成し、このやや大きめに形成したリード

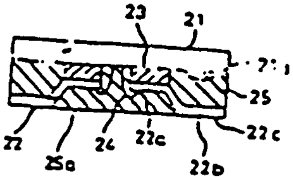
【図1】



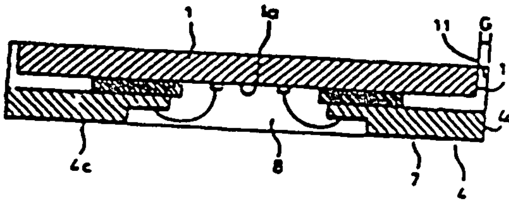
【図2】



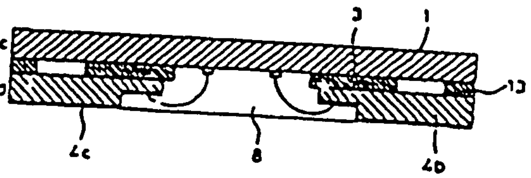
【図7】



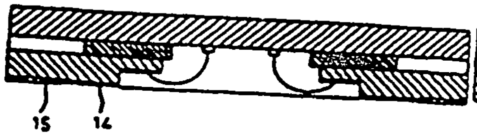
【図3】



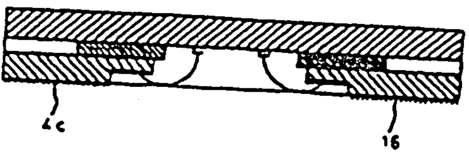
【図4】



【図5】



【図6】



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[TITLE OF THE INVENTION]

Semiconductor Device

[CLAIMS]

1. A semiconductor device including a semiconductor chip, a lead frame having a size substantially equal to that of the semiconductor chip, the lead frame being bonded to a surface of the semiconductor chip by an adhesive layer interposed therebetween under the condition in which the lead frame is overlapped with the semiconductor chip, bonding wires adapted to bond inner leads included in the lead frame to the semiconductor chip, and a resin encapsulate adapted to encapsulate a region toward the surface of the semiconductor chip in such a fashion that it has a surface flush with a surface of each of outer leads included in the lead frame to expose the surface of the outer lead at the surface of the resin encapsulate, wherein each of the inner leads has a reduced thickness at a surface thereof in such a fashion that the bonding wire connected to the inner lead does not extend beyond the surface of an associated one of the outer leads, whereby the surface of the inner lead is lower than the surface of the outer lead by one step.

2. The semiconductor device in accordance with claim 1, wherein the size of the lead frame is slightly larger than that of the semiconductor chip, and the resin encapsulate fills a gap defined between corresponding end surfaces of the semiconductor chip and the lead frame when the lead frame is laid on the surface of the semiconductor chip in an overlapped state.

3. The semiconductor device in accordance with claim 1 or 2, wherein the adhesive layer is disposed not only at a region where the inner leads are arranged, but also at a region where the outer leads are arranged.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a semiconductor device using a lead frame, and more particularly to a semiconductor package having a thin and compact structure substantially equal in size to a semiconductor chip packaged therein.

[DESCRIPTION OF THE PRIOR ART]

In DRAMs (Dynamic Random Access Memories) having a large capacity, an LOC (Lead On Chip) structure is mainly used which is capable of allowing a semiconductor chip having a large size to be packaged in a relatively small package, in order to meet a requirement of high-density mounting. However, the recent demand of an increased capacity has resulted in a requirement of compact semiconductor packages having a size reduced to a chip size level. Similarly, semiconductor packages for electronic appliances such as facsimile machines, personal computers, IC cards, and the like has been required to have a more compact structure in pace with the recent trend of those electronic appliances toward a compactness. Furthermore, such a compactness of a semiconductor package have been required with regard to not only the area occupied by the semiconductor package, but also the thickness of the semiconductor package.

In order to meet such requirements, a semiconductor device has been proposed which is called a "CSP (Chip Scale Package)" (Japanese Patent Laid-open Publication No. Heisei 6-132453). In such a CSP package, each lead is partially exposed at the lower surface of the package. Referring to Fig. 7 illustrating a detailed structure of this CSP package, a lead frame 22 having the same size as that of a semiconductor chip 21 is bonded to the wiring surface of the semiconductor chip 21, that is, the surface 21a, in such a fashion that their corresponding edges are aligned with each other, by means of an adhesive 23. Inner leads 22a of the lead frame 22 are connected to the semiconductor chip 21 by means of bonding wires 24. In this state, an encapsulating process is carried out using a molding resin 25. In this encapsulating process, the semiconductor chip 21 is encapsulated by the molding resin 25 at its portion toward its surface 21a, thereby causing the surface 22c of each outer lead 22b to be exposed at the surface 25a of the molding resin 25.

In this case, it is necessary to provide a stepped lead structure in order to prevent the bonding wires 24 serving to connect the inner leads 22a to the semiconductor chip 21 from being protruded from the surface 25a of the resin 25 flush with the surfaces 22c of the outer leads 22b. To this end, in this conventional example, the lead frame 22 is subjected to a down-setting process so that each inner lead 22a is lower than an associated one of the outer leads 22c by one step.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

In accordance with the above mentioned conventional technique, compactness of a semiconductor package can be achieved with regard to not only the area occupied by the semiconductor package, but also the thickness of the semiconductor package. However, since this technique provides a stepped lead structure by down-setting the lead frame, it requires a machining depth exceeding the lead thickness. For this reason, it is impossible to produce a package having a thickness less than the machining depth.

Where the semiconductor chip 1 has the same size as that of a package to be produced, the package may have a minimized size. However, if the semiconductor chip 1 has a non-uniform size, it may be damaged by a mold during an encapsulating process using the molding resin.

Furthermore, the lead frame may be in a state insufficiently fixed in a thickness direction at its portion near the outer leads during the encapsulating process because the bonding and fixing of the lead frame to the semiconductor chip is achieved at a portion of the lead frame near the inner leads. As a result, the molding resin may spread in the form of a thin film on the outer lead surface. In this case, it is necessary to shave off the resin film coated on the outer lead surface.

An object of the invention is to solve the above mentioned problems involved in the prior art, and to provide a semiconductor device having a reduced package thickness. Another object of the invention is to provide a semiconductor device having a structure capable of preventing its semiconductor chip from being damaged during an encapsulating process using a molding resin. Another object of the invention is to provide a semiconductor device having a structure capable of eliminating a requirement for its outer lead surface to be shaved off after an encapsulating process.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

The present invention provides a semiconductor device including a semiconductor chip, a lead frame having a size substantially equal to that of the semiconductor chip, the lead frame being bonded to a surface of the semiconductor chip by an adhesive layer interposed therebetween under the condition in which the lead frame is overlapped with the semiconductor chip, bonding wires adapted to bond inner leads included in the lead frame to the semiconductor chip, and a resin encapsulate adapted to encapsulate a region toward the surface of the semiconductor chip in such a fashion that it has a surface flush with a surface of each of outer leads included in the lead frame to expose the surface of the outer lead at the surface of the resin encapsulate, wherein each of the inner leads has a reduced thickness at a surface thereof in such a fashion that the bonding wire connected to the inner lead does not extend beyond the surface of an associated one of the outer leads, whereby the surface of the inner lead is lower than the surface of the outer lead by one step.

In the semiconductor device of the present invention, the size of the lead frame may be slightly larger than that of the semiconductor chip. In this case, the resin encapsulate fills a gap defined between corresponding end surfaces of the semiconductor chip and the lead frame when the lead frame is laid on the surface of the semiconductor chip in an overlapped state. Accordingly, it is possible to effectively prevent the semiconductor chip from being damaged. The adhesive layer may be disposed not only at a region where the inner leads are arranged, but also at a region where the outer leads are arranged. In this case, it is possible to prevent the molding resin from spreading on the outer lead surface.

[PREFERRED EMBODIMENTS OF THE INVENTION]

Hereinafter, preferred embodiments of the present invention will be described in detail in conjunction with the annexed drawings. Fig. 1 is a cross-sectional view illustrating a CSP structure in which a lead frame 4 having the same size of a semiconductor chip 1 is bonded to the semiconductor chip 1.

The semiconductor chip 1 is provided at its wiring surface, namely, a surface 1a, with bonding pads 2. These bonding pads 2 are arranged in the vicinity of the central portion of the surface 1a. The lead frame 4, which is attached to the surface 1a of the semiconductor chip 1, has the same size as that of the semiconductor chip 1. The lead frame 4 includes inner leads 4a adapted to come into contact with the semiconductor chip 1, and outer leads 4b each serving as an external terminal. The attachment between the semiconductor chip 1 and lead frame 4 is achieved by overlapping the semiconductor chip 1 and lead frame 4 with each other in such a fashion that each end surface 1c of the semiconductor chip 1 is aligned with an associated one of end surfaces 4d of the lead frame 4, and interposing a double-sided adhesive tape 3 between the overlapped semiconductor chip 1 and lead frame 4.

The lead frame 4 has a structure not bent, but having a reduced thickness at a desired portion thereof. That is, each inner lead 4a has a coining portion 5 having a thickness less than that of an associated one of the outer leads 4b. The coining portion 5 is formed by coining a surface of the inner lead 4a opposite to the bonding surface of the inner lead 4a, that is, a surface 4c. Accordingly, bonding wires 9, which connect the inner leads 4a to bonding pads 2 of the semiconductor chip 1 respectively, have a height lower than a surface of each outer lead 4b opposite to the bonding surface of the outer lead 4b, that is, the surface 4c.

For the coining portion 5 of each inner lead 4a arranged at a level lower than the surface 4c of the associated outer lead 4b by virtue of the above mentioned thickness reduction, a silver plating process is conducted to form a silver plating film 6. The coining portions 5 formed with the silver plating films 6 are connected with the bonding pads 2 arranged near the central portion of the semiconductor chip 1 by means of the bonding wires 9, respectively. Since each coining portion 5 is arranged at a level lower than the surface 4c of the associated outer lead 4b by one step, the associated bonding wire 9 can be controlled to have a height lower than the surface 4c of the outer lead 4b.

An encapsulating process using a molding resin is conducted at a region toward the surface 1a of the semiconductor chip 1, thereby forming a resin encapsulate 8. The thickness of the resin encapsulate 8 is determined in such a fashion that the resin encapsulate 8 is flush with the surfaces 4c of the outer leads 4b at its surface 8a. The inner leads 4a and bonding wires 9 are encapsulated by the resin encapsulate 8 so that they are protected. The surfaces 4c of the outer leads 4b are exposed at the surface 8a of the resin encapsulate 8. In order to reduce the area of the package while reducing the thickness of the package, the resin encapsulate 8 is prevented from extending beyond each end surface 4d of the lead frame 4, each end surface 1c of the semiconductor chip 1c, and the surface 1b of the semiconductor chip 1.

Since the semiconductor package configured as mentioned above has a stepped lead structure formed using a coining process, it is unnecessary for its lead frame to be down-set. The semiconductor package has a thickness corresponding to the sum of the thickness of the semiconductor chip, the thickness of the double-sided adhesive tape, and the thickness of one lead sheet. The thickness of the semiconductor package can be minimized because the lead portion of the semiconductor package involves no machining depth, corresponding to at least two times the lead thickness, required in a down-set structure.

In the fabrication of the above mentioned semiconductor package, the lead frame 4 used to fabricate the semiconductor package is arranged with respect to the semiconductor chip 1 in such a fashion that its resin dam bars 17 extend along the peripheral edges of the semiconductor chip 1 indicated by dotted lines in Fig. 2, so as to align each end surface 8b of the resin encapsulate 8 with the associated end surface 1c of the semiconductor chip 1. The mold used in the fabrication of the semiconductor package has a size substantially equal to the size of the semiconductor chip 1. The resin encapsulate 8 is molded only at a region toward the surface 1a of the semiconductor chip 1 while being prevented from spreading on the surface 1b of the semiconductor chip 1. Each resin dam bar 17 is cut along the associated end surface 4d of the lead frame 4.

After molding, the resin dam bars 17 are cut from the mold, thereby achieving a separation of the leads 4a and 4b. It is desirable that, prior to the cutting of the resin dam bars 17, a silver plating film 7 providing a good flowability of solder is formed on the surfaces 4c of the outer leads 4b exposed at the surface 8a of the resin encapsulate 8. The formation of the silver plating film 7 may be conducted simultaneously with the formation of the silver plating film 6 on the coining portions 5 of the inner leads 4a. In this case, it is unnecessary to conduct an external solder plating process for the surfaces of the outer leads 4b. Accordingly, it is possible to reduce the costs. Also, there is an advantage in that the number of processes, which may damage the package after the completion of the molding process, is reduced.

In accordance with the fabrication method according to the present invention, it is possible to use the fabrication process for LOC lead frames and the resin molding process associated therewith as they are or while partially eliminating them. Therefore, it is possible to obtain a package having a more compact and thinner structure while being equivalent in costs, as compared to conventional molded packages.

In the semiconductor package structure shown in Fig. 1, however, if the semiconductor chip 1 has a deviation in size, the mold may then damage a part of the semiconductor chip 1. This is because the package has the same size as the semiconductor chip 1 at its molding region. Such a problem can be eliminated by setting the molding region to have a size slightly larger than that of the semiconductor chip 1. Where the lead frame 4 is fabricated to have a size slightly larger than that of the semiconductor chip 1, and the mold is constructed to have a size corresponding to a region defined by the resin dam bars 17 defining the slightly increased size of the lead frame 4, the mold does not come into contact with the end surfaces 1c of the semiconductor chip 1 even when the semiconductor chip 1 has a deviation in size. Accordingly, it is possible to prevent the semiconductor chip 1 from being damaged. Although there is a gap G defined between each end surface 4d of the lead frame 4 and the associated end surface 1c of the semiconductor chip 1, this gap G is filled with the molding resin 11 during the formation of the resin encapsulate 8. Thus, the end surfaces 1c of the semiconductor chip 1 are protected by the mold resin 11 after the formation of the resin encapsulate 8.

Furthermore, in the semiconductor package structure shown in Figs. 1 and 3, if the lead frame is in a state insufficiently fixed in a thickness direction at its portion near the outer leads 4b by the double-sided adhesive tape 3 arranged at the inner lead region during the encapsulating process, the molding resin may spread in the form of a thin film on the surface 4c of the outer leads 4b. In this case, it is necessary to shave off the resin film coated on the surface 4c. The phenomenon of the molding resin spreading on the outer lead surface 4c can be effectively prevented by interposing a double-sided adhesive tape 13 having the same thickness as the double-sided adhesive tape 3 between the semiconductor chip and the outer leads 4b in the vicinity of the periphery of the package. A combination of the structures shown in Figs. 3 and 4 may also be used.

Although the silver plating film 7 is formed over the entire portion of the surface 4c of each outer lead 4b in the structure of Fig. 1, 3 or 4, this may inevitably result in an increase in costs because of an increase in the amount of silver used. However, the amount of silver used can be reduced by reducing the area coated with the silver plating film, as indicated by the reference numeral 14 in Fig. 5. In this case, there is an advantage in regard to costs. The reference numeral 15 denotes an area plated with no silver plating film.

Fig. 6 illustrates an example in which a solder plating film 16 is formed on the surface 4c of each outer lead 4b. As described above, the formation of the solder plating film on the surface of the outer lead 4b inevitably involves an increase in the number of processes damaging the package. Of course, this is not avoided in the present invention.

In the above mentioned embodiment of the present invention, a semiconductor chip was used which has a thickness of 0.3 mm. The lead frame used has a thickness of 0.15 mm. Also, the double-sided adhesive tape has a total thickness of 0.05 mm. The inner leads were subjected to a coining process to have coining portions having a thickness of 0.075 mm. Although the coining process was used as a method for reducing the thickness of the inner leads, a half-etching process may be used. Although the double-sided adhesive tape was used as a means for attaching the semiconductor chip to the lead frame, an adhesive may be simply used.

[EFFECTS OF THE INVENTION]

In accordance with the present invention, a stepped lead structure is provided by a reduction in the thickness of each inner lead. Accordingly, it is unnecessary to give a machining depth exceeding the lead thickness. Such a machining depth is required in the conventional method in which a stepped lead structure is provided in accordance with a down-setting process. Thus, it is possible to produce a semiconductor package having a reduced thickness. Since the lead frame has a size slightly larger than that of the semiconductor chip in accordance with the present invention, it is possible to effectively prevent the semiconductor chip from being damaged by the mold.

Moreover, it is possible to prevent the molding resin from spreading on the surfaces of the outer leads because the adhesive adapted to bond the lead frame to the surface of the semiconductor chip is also applied to the outer leads. Accordingly, it is unnecessary to shave off the outer lead surfaces.

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mi conductor device with lead frame for high density mounting - has outer lead exposed sealing resin surface

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The device includes a semi conductor chip (1) bonded with a lead frame (4). The ad frame consists of an inner lead (4a) and an outer lead (4b).

A bonding wire (9) is used to bond the inner lead frame and the semi conductor hip. A mould resin (8) is sealed on the surface of the semi conductor chip. The main ody has outer lead exposed in a sealing resin surface (8a).

ADVANTAGE - Decreases package thickness. Prevents semi conductor chip from amage. (5pp Dwg.No.2/7)

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